REMARKS

Upon entry of the above amendments, claims 1-13, 21 and 22 will be pending. Applicants propose amendment of claim 1 and the addition of new claim 22. A marked-up version showing the proposed changes made by the present amendment is hereto attached as "**Version with markings to show changes made**."

As a preliminary matter, the Office Action indicates that an Information Disclosure Statement (PTO-1449) as an attachment. This attachment was not received with the Office Action.

Several errors in Form PTO-1449 have been noted. Specifically, document number AK was listed incorrectly by its application number. Furthermore, four references which had been cited in the related copending applications noted in the information disclosure statement were not listed. These documents include the following:

(1) "Physics of Semiconductor Devices Second Edition" by S.M. Sze, pp. 393, 1981.

(2) USP5,665,845 (Cited in S.N. 08/997,049)

(3) USP4,920,071 (Cited in S.N. 09/716,334)

(4) USP5,541,445 (Cited in S.N. 09/716,334)

Accordingly, a revised and corrected Form PTO-1449 is attached hereto. The changes on this form have been highlighted. Copies of the above documents are also attached for the Examiner's reference.

In addition, an information disclosure statement is filed herewith citing USP 5,459,086. This reference was cited in one of the related applications.

Claims 1-13 and 21 were rejected under 35 U.S.C. §102(e) as being anticipated by *Mizuhara et al.* or *Watanabe et al.* Favorable reconsideration of this rejection is earnestly solicited.

Amendment of claim 1 is proposed to specify "by the Damascene method." When the Damascene method used, the underlying face over the substrate must be flat over the whole substrate. Therefore, the first insulation layer is, as a matter of course, to be formed on the underlying face that is flat over the whole substrate. In contrast thereto, modified SOG films disclosed in *Mizuhara et al.* and *Watanabe et al.* are formed on the uneven underlying face which has steps of interconnections without exception.

The advantage of forming the modified SOG film on the flat underlying face over the whole substrate is disclosed in the present specification at page 9, line 12 through page 10, line 2.

Proposed new independent claim 22 also specifies this feature.

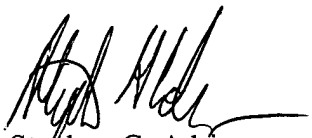
For at least the foregoing reasons, the claimed invention distinguishes over the cited art and defines patentable subject matter. Favorable reconsideration is earnestly solicited.

Should the Examiner deem that any further action by Applicants would be desirable to place the application in condition for allowance, the Examiner is encouraged to telephone Applicants' undersigned attorney.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN & HATTORI, LLP



Stephen G. Adrian
Attorney for Applicant
Reg. No. 32,878

SGA/arf
Atty. Docket No. **990559**
Suite 1000, 1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930

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PATENT TRADEMARK OFFICE

Enclosures: Version with markings to show changes made
Corrected Form PTO-1449 w/ Copies of documents highlighted
Information Disclosure Statement

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VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/320,271

IN THE CLAIMS:

Claim 1 has been amended as follows:

1. **(Five Times Amended)** A fabrication method of a semiconductor device comprising the steps of:

forming a first insulation layer on a flat underlying face over a substrate,

introducing impurities into said first insulation layer, and

embedding and forming a first conductive layer in said first insulation layer by the Damascene method.